CLAIMS

1. A decision directed phase locked loop circuit, comprising:

a phase detector which receives an input sequence of baseband complex samples in a data communication system and a plurality of different phase/frequency estimates and generates phase differences between said baseband complex samples and said plurality of phase/frequency estimates;

an inner block decoder which decodes said baseband complex samples multiple times with different phase/frequency estimates to generate multiple decoded data;

a phase error generation circuit which receives said baseband complex samples and said decoded data from said inner block decoder and which generates multiple feedback phase error terms based on said baseband complex samples and said multiple decoded data;

a selection circuit which selects one of said multiple feedback phase error terms based on said baseband complex samples or selects one of said multiple decoded data;

an outer block decoder which receives the associated codewords generated by said inner block decoder based on the selection of said selection circuit;

a loop filter which filters said phase error terms; and

a phase accumulator that updates the current phase estimate on each iteration of the phase locked loop.

2. A decision directed phase locked loop as claimed in claim 1, wherein the baseband complex samples are demodulated from an input modulated signal corresponding to one of a binary phase shift keying (BPSK) modulated signal and a quaternary phase shift keying (QPSK) modulated signal and encoded by a sequence of codewords.

3. A decision directed phase locked loop as claimed in claim 2, wherein said codewords correspond to biorthogonal binary codes.

4. A decision directed phase locked loop as claimed in claim 3, wherein each of said codewords contains four data symbols, and the decode rate for decoding a set of vector pairs of phase stabilized observables corresponds to one quarter of a symbol rate.

5. A decision directed phase locked loop as claimed in claim 4, wherein said inner block decoder comprises a Reed-Muller block decoder.

6. A decision directed phase locked loop as claimed in claim 5, wherein said phase error generation circuit generates said feedback phase error terms based on the composite decoded codeword phase error relative to reference.

7. A decision directed phase locked loop as claimed in claim 6, wherein said current phase estimate is updated at one quarter the symbol rate.

8. A decision directed phase locked loop as claimed in claim 6, wherein said current phase estimate is updated every codeword of four data symbols.

9. A decision directed phase locked loop as claimed in claim 1, wherein said phase detector includes a subtractor for subtracting the incoming phase of said baseband complex samples from the current phase estimate to generate said phase differences.

10. A demodulator for demodulating a modulated signal in a data communication system, comprising:

a phase locked loop having a first block decoder configured to decode a set of vector pairs of the input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate, wherein said set of vector pairs input data is processed multiple times with different initial phase and frequency estimates to calculate a plurality of phase/frequency error estimates;

a selection circuit which receives the plurality of phase/frequency estimates from the phase locked loop and selects one phase/frequency error estimate from among the plurality of phase/frequency error estimates; and

a second block decoder which receives the phase/frequency estimate selected by said selection circuit and corrects errors in the set of associated codewords using the selected phase/frequency estimate.

11. A demodulator as claimed in claim 10, wherein said first block decoder also generates reliability metric results.

12. A demodulator as claimed in claim 11, wherein said reliability metric results comprise correlation results taken during decoding by said first block decoder.

13. A decoder as claimed in claim 11, wherein said second block decoder selects codewords from said set of associated codewords based on the reliability metric results from said first block decoder.

14. A demodulator as recited in claim 10, wherein said block decoder comprises a Reed-Muller block decoder.

15. A demodulator as claimed in claim 14, wherein said Reed-Muller block decoder determines the phase error estimate based on the composite decoded codeword phase error relative to reference.

16. A demodulator as claimed in claim 15, wherein said second block decoder preselects the codewords from among said set of associated codewords.

17. A demodulator as claimed in claim 16, wherein said preselected codewords comprises the first codewords of the set of associated codewords.

18. A communication receiver using a demodulator demodulating an input modulated signal from a transmission channel which is encoded by a sequence of codewords, comprising:

a plurality of phase locked loops which provide respective estimates of the phase of said input modulated signal, each one of said phase locked loops receiving the input modulated signal and calculating a phase estimate using a different combination of frequency and initial phase estimate and comprising a first block decoder which decodes the set of vector pairs of said input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate;

a selection circuit which receives the phase/frequency estimates from each one of the phase locked loops and selects one phase/frequency error estimate from among the plurality of phase/frequency error estimates; and

a second block decoder which receives the phase/frequency estimate selected by said selection circuit and corrects errors in the set of associated codewords using the selected phase/frequency estimate.

19. A communication receiver as claimed in claim 18, wherein said input modulated signal comprises a phase shift keying modulated signal.

20. A communication receiver as claimed in claim 18, wherein said first block decoder in each phase locked loop also generates reliability metric results.

21. A communication receiver as claimed in claim 20, wherein said reliability metric results comprise correlation results taken during decoding by said first block decoders.

22. A communication receiver as claimed in claim 20, wherein said second block decoder dynamically selects codewords from said set of associated codewords based on the reliability metric results from the corresponding first block decoder.

23. A communication receiver as claimed in claim 18, wherein said first block decoders are Reed-Muller block decoders.

24. A communication receiver as claimed in claim 23, wherein said block decoders determine the phase error estimate based on the composite decoded codeword phase error relative to reference.

25. A communication receiver as claimed in claim 24, wherein said second block decoder preselects the codewords from among said set of associated codewords.

26. A communication receiver as claimed in claim 25, wherein said preselected codewords comprise the first codewords of the set of associated codewords.

27. A communication receiver as claimed in claim 19, wherein said down converter down converts said input modulated signal into an intermediate frequency signal, and wherein said communication receiver further comprises:

a synchronous demodulator which demodulates said intermediate frequency signal from a baseband quadrature pair into a sequence of complex sample pairs; and

a matched filter and sampler which passes said sequence of complex sample pairs and samples at a symbol rate to produce said succession of baseband signal samples.